

Name of Subject : Digital Electronics

Semester : 3rd

Name of faculty : Vivek dalal

Branch : computer(Programmer)

| week | Lecture | Name of Topic | Practical |
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| 1st | 1 st | Introduction to Digital Electronics, Distinction between analog and digital signal. | Introduction with digital Lab equipments |
| | 2 nd | Applications and advantages of digital signals | |
| | 3rd | Binary, octal and hexadecimal number system: conversion from decimal and hexadecimal to binary and vice-versa. | |
| 2nd | 4th | Binary addition and subtraction including binary points. 1's and 2's complement method of addition/subtraction. | Verification and interpretation of truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and Exclusive NOR(EXNOR) gates |
| | 5th | Concept of code, weighted and non-weighted codes, examples of 8421, BCD, excess-3 and Gray code. | |
| | 6th | Concept of parity, single and double parity and error detection. | |
| 3rd | 7th | Concept of negative and positive logic | Realisation of logic functions with the help of NAND or NOR gates |
| | 8th | Definition, symbols and truth tables of NOT, AND, OR, NAND, NOR, EXOR Gates, | |
| | 9th | NAND and NOR as universal gates. | |
| 4 th | 10th | Introduction to TTL and CMOS logic families | Practical checking and viva-voce |
| | 11th | Revision | |
| | 12 th | Logic simplification | |
| 5 th | 13 th | Postulates of Boolean algebra, De Morgan's Theorems. | To design a half adder using XOR and NAND gates and verification of its operation |
| | 14 th | Implementation of Boolean (logic) equation with gates | |
| | 15th | Karnaugh map (upto 4 variables) and simple application in developing combinational logic circuits. | |
| 6th | 16 th | Test and assignment | Construction of a full adder circuit using XOR and NAND gates and verify its operation |
| | 17th | K-Map Practice | |
| | 18 th | Half adder, design and implementation. | |
| 7 th | 19th | and Full adder circuit , design and implementation and 4 bit adder circuit | Verification of truth table for encoder and decoder ICs, Mux and De-Mux |
| | 20 th | Basic functions and block diagram of MUX and DEMUX with different ICs. | |
| | 21 st | Four bit decoder circuits for 7 segment display and decoder/driver ICs. | |

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| 8th | 22 nd | Basic functions and block diagram of Encoder | Practical checking and viva-voce |
| | 23 rd | Concept and types of latch with their working and applications | |
| | 24 th | Difference between a latch and a flip flop | |
| 9th | 25 th | Operation using waveforms and truth tables of RS, T, D, | Verification of truth table for positive edge triggered, negative edge triggered, level triggered IC flip-flops (At least one IC each of D latch, D flip-flop, JK flip-flops). |
| | 26 th | Master/Slave JK flip flops. | |
| | 27 th | Introduction to Asynchronous and Synchronous counters. | |
| 10th | 28 th | Binary counters | Use of Asynchronous Counter ICs (7490 or 7493) |
| | 29 th | Divide by N ripple counters. | |
| | 30 th | Decade counter. | |
| 11 th | 31 st | Ring counter | |
| | 32 nd | Revision | |
| | 33 rd | Test and assignment | |
| 12th | 34 th | Introduction and basic concepts including shift left and shift right. Serial in parallel out, serial in serial out, | To design a 4 bit ring counter and verify its operation. |
| | 35 th | parallel in serial out, parallel in parallel out. | |
| | 36 th | Universal shift register | |
| 13 th | 37 th | Working principle of A/D and D/A converters Brief idea about different techniques of A/D conversion | To design a 4 bit SISO, SIPO, PISO, PIPO shift registers using JK/D flip flops and verification of their operation |
| | 38 th | Detail study of Binary Weighted D/A converter. | |
| | 39 th | R/2R ladder D/A converter | |
| 14 th | 40 th | Stair step Ramp A/D converter, Dual Slope A/D converter | Viva |
| | 41 st | Successive Approximation A/D Converter Applications of A/D and D/A converter. | |
| | 42 nd | Memory organization,. | |
| 15th | 43 rd | classification of semiconductor memories (RAM, ROM, PROM, EPROM, EEPROM), static and dynamic RAM, | Viva |
| | 44 th | Introduction to 74181 ALU IC | |
| | 45 th | Test and assignment | |