Government Polytechnic, mandi Adampu			
Name of Faculty: Sh. Balinder Singh			
Discipline: Electronics			
Semester: 3			
Subject: DIGITAL ELECTRONICS			
Lesson Plan Duration: 18 Week			
Week	**Theory**		
	Lecture Day	**Topic**	**Practical Day**
Week 1	Day 1	**Unit 1 Introduction:** a) Distinction between analog and digital signal.	day 1
	Day 2	b) Applications and advantages of digital signals.	
	Day 3	**Test Unit 1**	
Week 2	Day 4	**Unit 2 Number System:** a) Binary, octal and hexadecimal number system: conversion from decimal	day 2
	Day 5	and hexadecimal to binary and vice-versa.	
	Day 6	b) Binary addition and subtraction including binary points. 1's and 2's complement method of addition/subtraction.	
Week 3	Day 7	**Test Unit 2**	day 3
	Day 8	**Unit 3 Codes and Parity:** a) Concept of code, weighted and non-weighted codes, examples of 8421	
	Day 9	BCD, excess-3 and Gray code.	
Week 4	Day 10	b) Concept of parity, single and double parity and error detection	day 4
	Day 11	**Test Unit 3**	
	Day 12	**Unit 4 Logic Gates and Families:** a) Concept of negative and positive logic	
Week5	Day 13	b) Definition, symbols and truth tables of NOT, AND, OR, NAND,	day 5
	Day 14	NOR, EXOR Gates,	
	Day 15	NAND and NOR as universal gates.	
Week 6	Day 16	c) Introduction to TTL and CMOS logic families	day 6
	Day 17	**Test Unit 4**	
	Day 18	**Unit 5 Logic Simplification:** a) Postulates of Boolean algebra, De Morgan's Theorems.	

Week 7	Day 19	Implementation of Boolean (logic) equation with gates	day 7
	Day 20	b) Karnaugh map (upto 4 variables)	
	Day 21	and simple application in developing combinational logic circuits	
Week 8	Day 22	**test unit 5**	day 8
	Day 23	**Unit 6 Arithmetic circuits :** a) Half adder and Full adder circuit, design and implementation.	
	Day 24	b) 4 bit adder circuit	
	Day 25	**Test unit 6**	day 9
	Day 26	**Unit 7: Decoders, Multiplexeres, Multiplexeres and Encoder** a) Four bit decoder circuits for 7 segment display and decoder/driver ICs**.**	
	Day 27	b) Basic functions and block diagram of MUX	
Week 10	Day 28	and DEMUX with different ICs	day 10
	Day 29	c) Basic functions and block diagram of Encoder	
	Day 30	**Test Unit 7**	
Week 11	Day 31	**Unit 8 Latches and flip flops:** a) Concept and types of latch with their working and applications	day 11
	Day 32	b) Operation using waveforms and truth tables of RS, T, D	
	Day 33	Master/Slave JK flip flops.	
Week 12	Day 34	c) Difference between a latch and a flip flop	day 12
	Day 35	**Test Unit 8**	
	Day 36	**unit 9 Counters:** a) Introduction to Asynchronous and Synchronous counters	
Week 13	Day 37	b) Binary counters	day 13
	Day 38	c) Divide by N ripple counters,	
	Day 39	Decade counter	
Week 14	Day 40	Ring counter	day 14
	Day 41	**test Unit 9**	
	Day 42		
	Day 42	**Unit 10 Shift Register:** Introduction and basic concepts including shift left and shift right	
Week 15	Day 43	a) Serial in parallel out, serial in serial out,	day 15

	Day 44	parallel in serial out, parallel in parallel out.	
	Day 45	b) Universal shift register	
Week 16	Day 46	**test Unit 10**	day 16
	Day 47	**Unit 11 A/D and D/A Converters:** Working Principle of A/D and D/A converters	
	Day 48	- Brief idea about different techniques of A/D conversion and study of • Stair step Ramp A/D converter • Dual Slope A/D converter	
Week 17	Day 49	• Successive Approximation A/D Converter	day 17
	Day 50	• Binary Weighted D/A converter • R/2R ladder D/A converter	
	Day 51	**test Unit 11**	
Week 18	Day 52	**Unit 12 Semiconductor Memories:** Memory organization, classification of semiconductor memories (RAM, ROM, PROM, EPROM, EEPROM),	day 18
	Day 53	static and dynamic RAM, introduction to 74181 ALU IC	
	Day 54	**test Unit 12**	

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Practical
Topic
Verification and interpretation of truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and Exclusive NOR(EXNOR) gates
File Check
Realisation of logic functions with the help of NAND or NOR gates
File Check
To design a half adder using XOR and NAND gates and verification of its operation - Construction of a full adder circuit using XOR and NAND gates and verify its
File Check

Verification of truth table for positive edge triggered, negative edge triggered, level triggered IC flip-flops (At least one IC each of D latch , D flip-flop, JK flip-flops).
File Check
Verification of truth table for encoder and decoder ICs, Mux and DeMux
File Check
To design a 4 bit SISO, SIPO, PISO, PIPO shift registers using JK/D flip flops and verification of their operation.
File Check
To design a 4 bit ring counter and verify its operation.
File Check
8. Use of Asynchronous Counter ICs (7490 or 7493)

File Check