## GOVT. POLYTECHNIC MANDI ADAMPUR

LESSON PLAN			
Name of the			
Faculty:	Raj Kumar		
Discipline:	COMPUTER ENGINEERING		
Semester	<b>4</b> тн		
Subject	COMPUTER ORGANIZATION		
Lesson Plan			
Duration	16 WEEKS		

\*\* Work Load (Lecture/ Practical)per week (in hours) : Lecture-04 Practical-0

WEE K			Theory			
		Lectur e Day	Topic ( Including Assignment and Test			
lst		lst	A brief over view of the subject "Computer organization " and relevance of the studying the subject in Diploma level Program.			
		2nd	CPU Organization : Concept of Registers and General Register Organization			
		3rd <b>4</b> th	Concept of Stack Organization Concept of Instruction Format and types of instructions			
2nd	lzc	5 <sup>th</sup> 6 <sup>th</sup>	Concept of Three Address instruction Concept of Two Address instruction			
		7th 8th	Concept of One Address instruction Concept of Zero Address instruction			
3rd		9th	Concept of RICS instruction			

	$10^{\text{th}}$	Revision of Lectures 1 <sup>st</sup> to 9th	
	11 <sup>th</sup>	Pre Sessional Class Test -1 (Syllabus content of Lectures 1 <sup>st</sup> to 9 <sup>th</sup> )	
	12 <sup>th</sup>	Concept of CPU Design	
4th	13 <sup>th</sup>	Concept of Micro programmed controlled	
	14 <sup>th</sup>	Concept of Hard wired controlled	

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		1 -	Concept of Reduced instruction Set
5 <sup>th</sup>		15 <sup>th</sup>	Computer
		5th16 <sup>th</sup>	
		17 <sup>th</sup>	RICS Characteristics
		18 <sup>th</sup>	Seminar on Topics , Instruction formats and Addressing modes , CICS, RICS
<b>6</b> <sup>th</sup>		19 <sup>th</sup>	<b>Revision of Lectures 12<sup>th</sup> to 17<sup>th</sup></b>
		20 <sup>th</sup>	Pre Sessional Class Test 2 (Syllabus content of Lectures 12th <sup>t</sup> to 17 <sup>th)</sup>
<b>7</b> th			Concept of Memory Organization,
		21st	Memory types
		22 <sup>nd</sup> 23 <sup>rd</sup>	Memory Hierarchy
		23 24 <sup>th</sup>	ROM and RAM Chips
		24	Concept of Memory Address Map
8th	-	25 <sup>th</sup>	Connections of Memory Chips with the CPU
U		26 <sup>th</sup>	Revision of Lecture 21 <sup>st</sup> to 25th
		27 <sup>th</sup>	Pre-sessional Class Test-1 Syllabus Content (Lecture 21 <sup>st</sup> to 25 <sup>th</sup> )
9 <sup>th</sup>	T	28 <sup>th</sup>	Concept and usage of Auxiliary Memories and types
a ot	-	29 <sup>th</sup>	Study of Magnetic Disks
10 <sup>t</sup>		30 <sup>th</sup>	Study of Magnetic Tapes.
	<b> </b>	31 <sup>st</sup>	Associative and Cache memory
		32nd	Concept of Virtual Memory
		33rd	Concept of Memory Management
		34 <sup>th</sup>	Memory Management Hardware.
t			Seminar topics: Memories and their
h	1	35 <sup>th</sup>	organization
h	-	36 <sup>th</sup>	organization Revision of Lecture 28 <sup>th</sup> to 34th
h		35 <sup>th</sup> 36 <sup>th</sup> 37 <sup>th</sup>	Revision of Lecture 28 <sup>th</sup> to 34th
h		36 <sup>th</sup>	organization Revision of Lecture 28 <sup>th</sup> to 34th Quiz contest Unit 1 and Unit 2 Pre-sessional Class Test-2 Syllabus Content (Lecture 28 <sup>th</sup> to 34 <sup>th</sup> ) Concept of Input/output Organization

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	12	ADA	MPU	R
	th		45 <sup>th</sup>	Concept of Synchronous and Asynchronous Data Transfer Modes
			46 <sup>th</sup>	Concept of Interrupt Initiated Data transfer modes
	13 <sup>th</sup>		47 <sup>th</sup>	Concept of Interrupt Initiated Data transfer odes .co ti ued
_	14	_	48 <sup>th</sup>	Concept of DMA and DMA Transfer mode of data .
	th		49th	Revision of Lectures 43 <sup>rd</sup> to 48th
			50 <sup>th</sup>	Pre Sessional Class Test Concept of Multi Processor Systems
			51 <sup>st</sup> 52 <sup>nd</sup>	Different forms of Parallel Processing
	15		53 <sup>rd</sup>	Differe t for s of Parallel Processi g continued
1	th		54 <sup>th</sup>	Concept of Parallel processing and Pipe Lines
			55 <sup>th</sup>	Basic Characteristics of Multiprocessor
	<sup>16</sup> th ⊣ ≦	56 <sup>th</sup> 57 <sup>th</sup> 58 <sup>th</sup>	General purpose multiprocessors. Concept of Interconnection Networks , Concept of Time Shared Common Bus	
		< _	59 <sup>th</sup>	Concept of Multiport Memory
			60 <sup>th</sup>	Cross Bar Switch , Multistance Cusitable and burger
			61 <sup>st</sup>	Multistage Switching networks and hyper cube structures
			62 <sup>nd</sup>	Compulsory Seminar (Syllabus Topics)
			63rd	Revision of Lectures 51 <sup>st</sup> to 61 <sup>st</sup> .
			64 <sup>th</sup> .	Pre Sessional Class Test